SPMICRO
三浦微电子

MU2N65

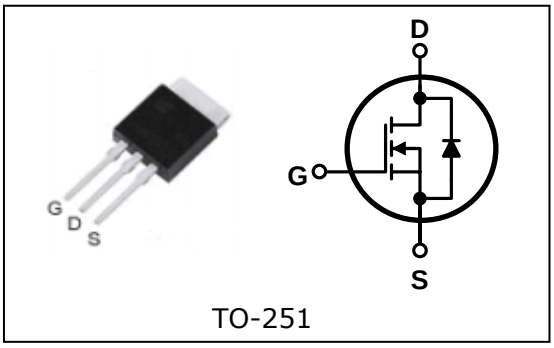
Power MOSFET

SWITCHING REGULATOR APPLICATIONS

Features

- High Voltage : BV_{DSS}=650V(Min.)
- Low C_{rss} : C_{rss}=7.6pF(Typ.)
- Low gate charge : Qg=15.3nC(Typ.)
- Low $R_{DS(on)}$: $R_{DS(on)}$=5.0Ω (Max.)

PIN Connection



TO-251

Ordering Information

Type No.	Marking	Package Code
MU2N65	MU2N65	TO-251

Absolute maximum ratings (T_C=25°C unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V_{DSS}		650	V
Gate-source voltage	V_{GSS}		±30	V
Drain current (DC) *	I_D	(Tc=25℃)	2.0	A
		(Tc=100℃)	1.3	A
Drain current (Pulsed) *	I_{DM}		6.0	A
Power dissipation	P_D		46	W
Avalanche current (Single) ②	I_{AS}		2.0	A
Single pulsed avalanche energy ②	E_{AS}		120	mJ
Avalanche current (Repetitive) ①	I_{AR}		2.0	A
Repetitive avalanche energy ①	E_{AR}		5.4	mJ
Junction temperature	T_J		150	°C
Storage temperature range	T_{stg}		-55~150	

* Limited by maximum junction temperature

Characteristic		Symbol	Typ.	Max.	Unit
Thermal resistance	Junction-case	$R_{th(J-C)}$	-	2.7	°C/W
	Junction-ambient	$R_{th(J-A)}$	-	62.5	

Electrical Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	I_D=250uA, V_{GS}=0	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	I_D=250uA, V_{DS}=V_{GS}	2.0	-	4.0	V
Drain-source cut-off current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-		10	uA
Gate leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
Drain-source on-resistance ④	$R_{DS(ON)}$	V_{GS}=10V, I_D =1A	-	4.2	5.0	Ω
Forward transfer conductance ④	g_{fs}	V_{DS}=50V, I_D=1A -		2.05		S
Input capacitance	Ciss	V_{GS}=0V, V_{DS}=25V, f=1MHz		380	490	pF
Output capacitance Coss -	Coss			35	46	
Reverse transfer capacitance	Crss		-	7.6	9.9	
Turn-on delay time	$t_{d(on)}$	V_{DD}=300V, I_D=2.0A R_G=25Ω ③④	-	5.5	-	ns
Rise time	t_r		-	16	40	
Turn-off delay time	$t_{d(off)}$		-	40	90	
Fall time	t_f		-	40	90	
Total gate charge	Q_g	V_{DS}=320V, V_{GS}=10V I_D=2.0A ③④	-	15.3	19	nC
Gate-source charge	Q_{gs}		-	1.8		
Gate-drain charge	Q_{gd}		-	7.2	-	

Source-Drain Diode Ratings and Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	2.0	A
Source current (Pulsed) ①	I_{SM}		-	-	6.0	
Forward voltage ④	V_{SD}	V_{GS}=0V, I_S=1.0A	-	-	1.4	V
Reverse recovery time	t_{rr}	I_S=1.0A, V_{GS}=0V dI_F/dt=100A/us	-	250	-	ns
Reverse recovery charge	Q_{rr}		-	1.31	-	uC

Note ;

① Repetitive rating : Pulse width limited by maximum junction temperature

② L=1080mH, I_{AS}=0.3A, V_{DD}=50V, R_G=25Ω, Starting T_J=25℃

③ Pulse Test : Pulse width≤300us, Duty cycle≤2%

④ Essentially independent of operating temperature

Electrical Characteristic Curves

Fig. 1 I_D - V_{DS}

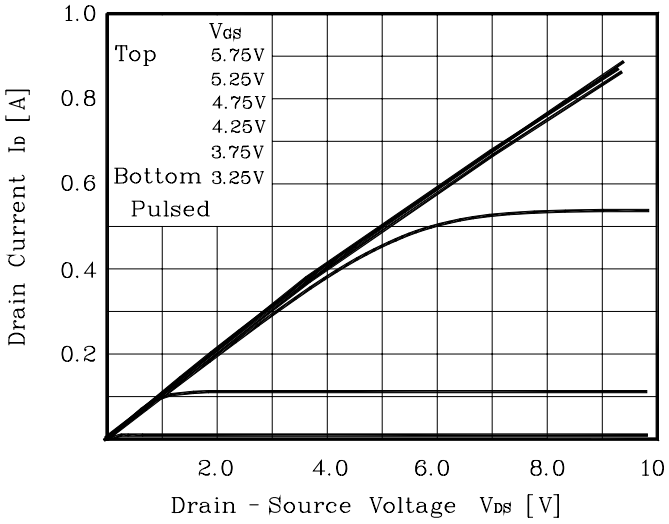


Fig. 2 I_D - V_{GS}

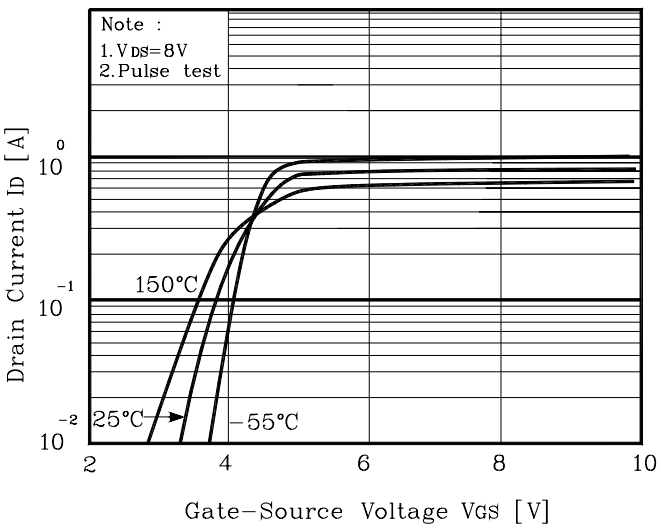


Fig. 3 $R_{DS(on)}$ - I_D

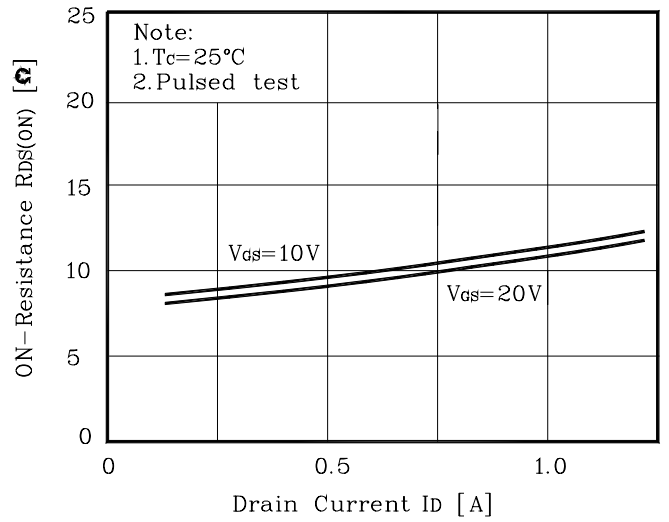


Fig. 4 I_S - V_{SD}

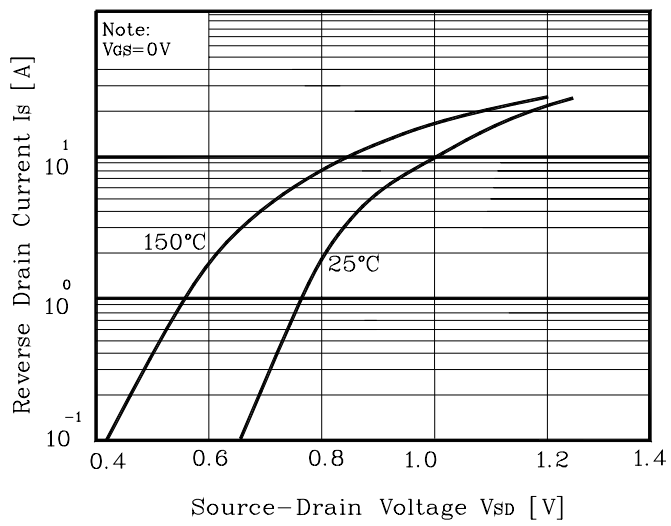


Fig. 5 Capacitance - V_{DS}

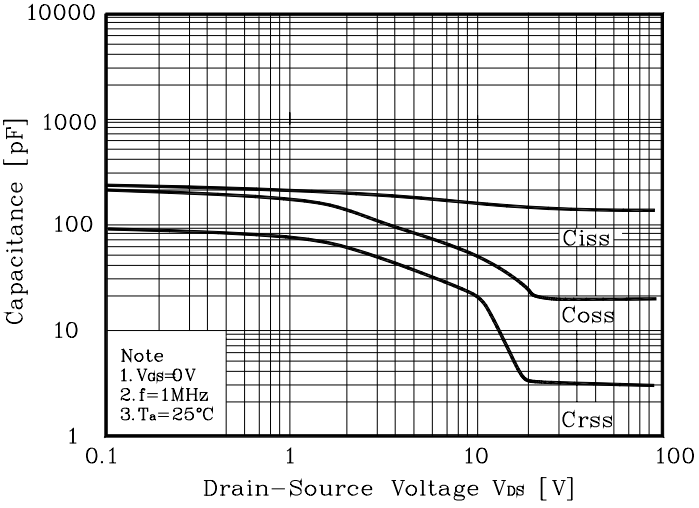


Fig. 6 V_{GS} - Q_G

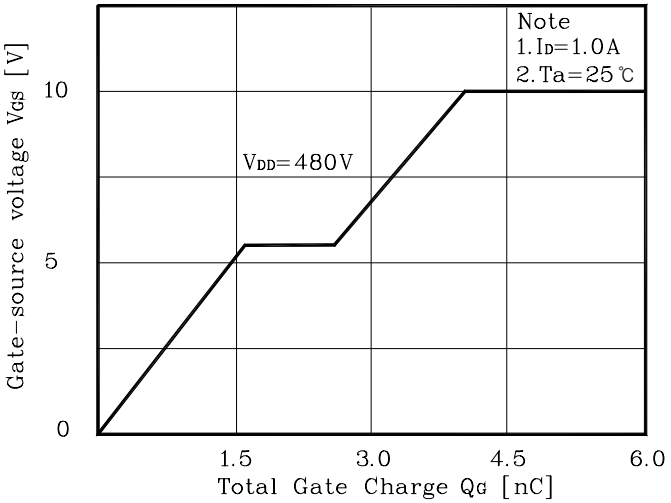


Fig. 7 V_{DSS} - T_J

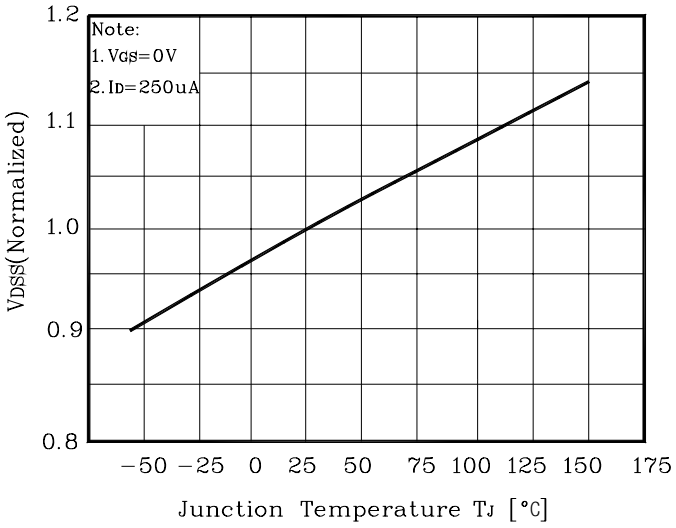


Fig. 8 $R_{DS(on)}$ - T_J

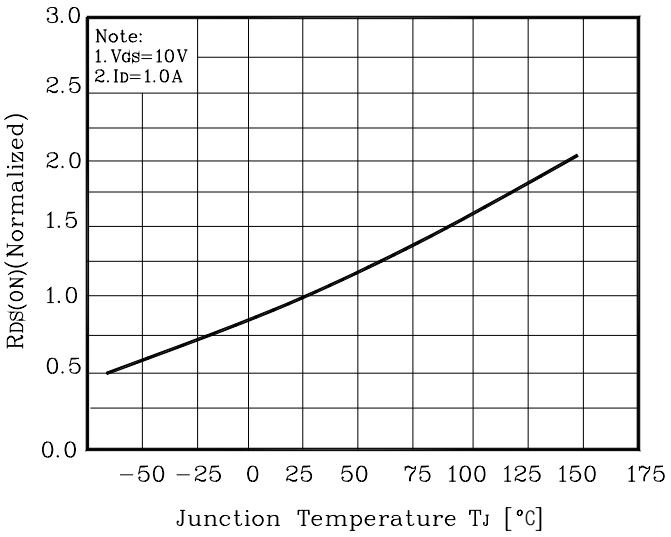


Fig. 9 I_D - T_a

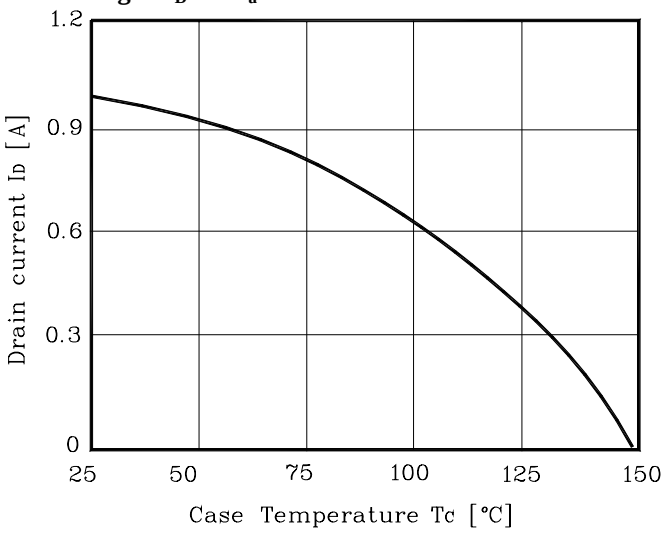


Fig. 10 Safe Operating Area

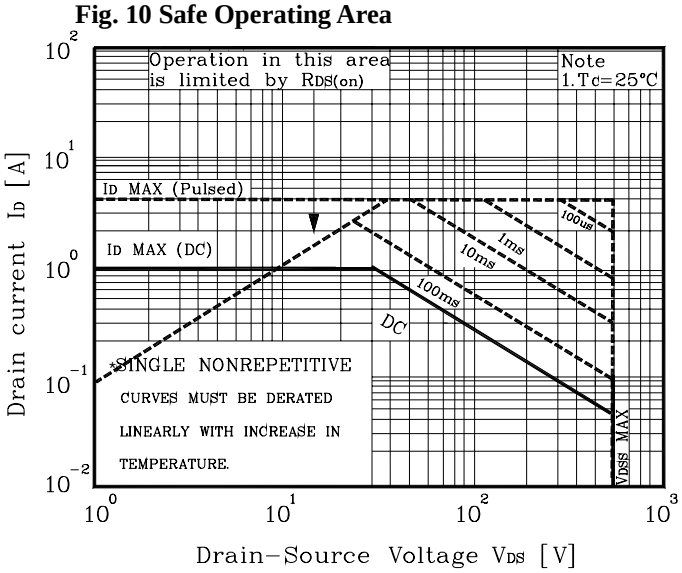


Fig. 11 Gate Charge Test Circuit & Waveform

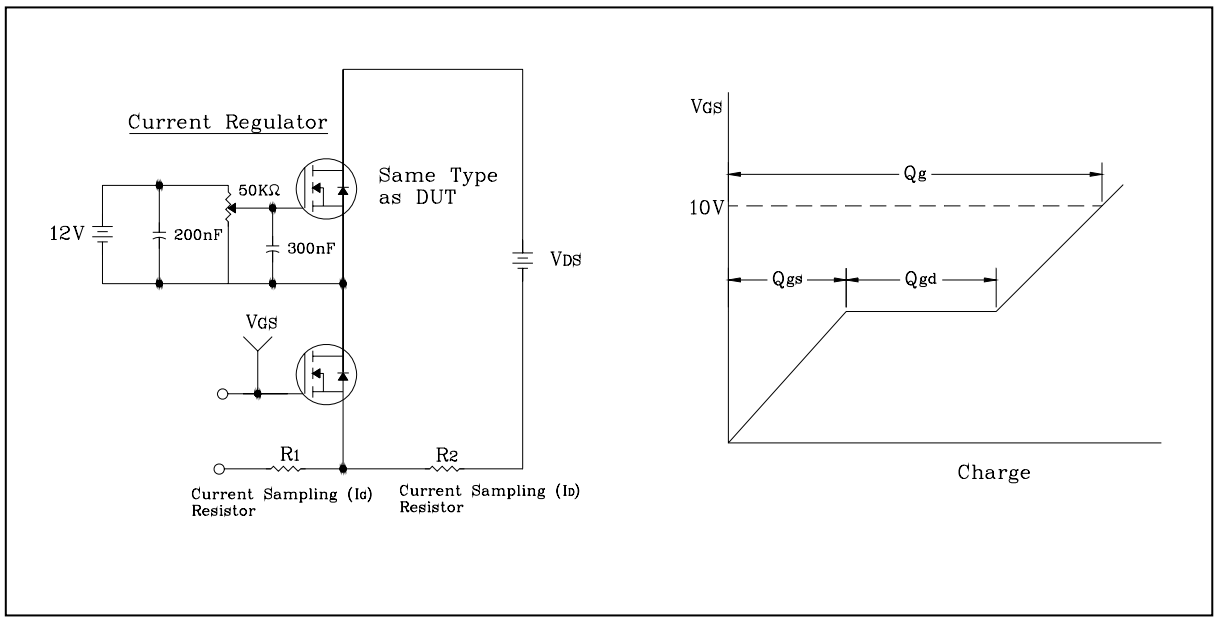


Fig. 12 Resistive Switching Test Circuit & Waveform

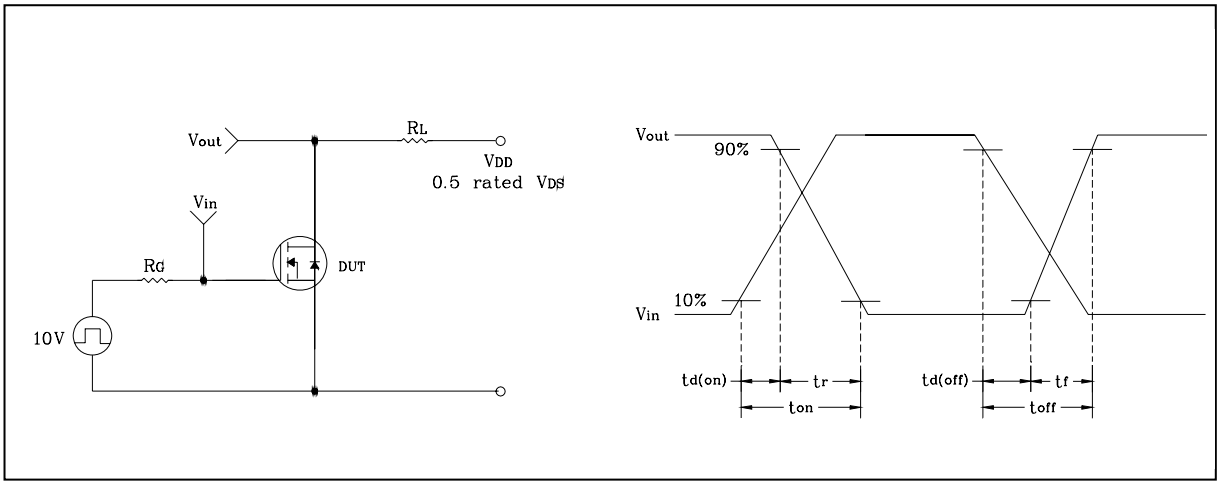


Fig. 13 E_{AS} Test Circuit & Waveform

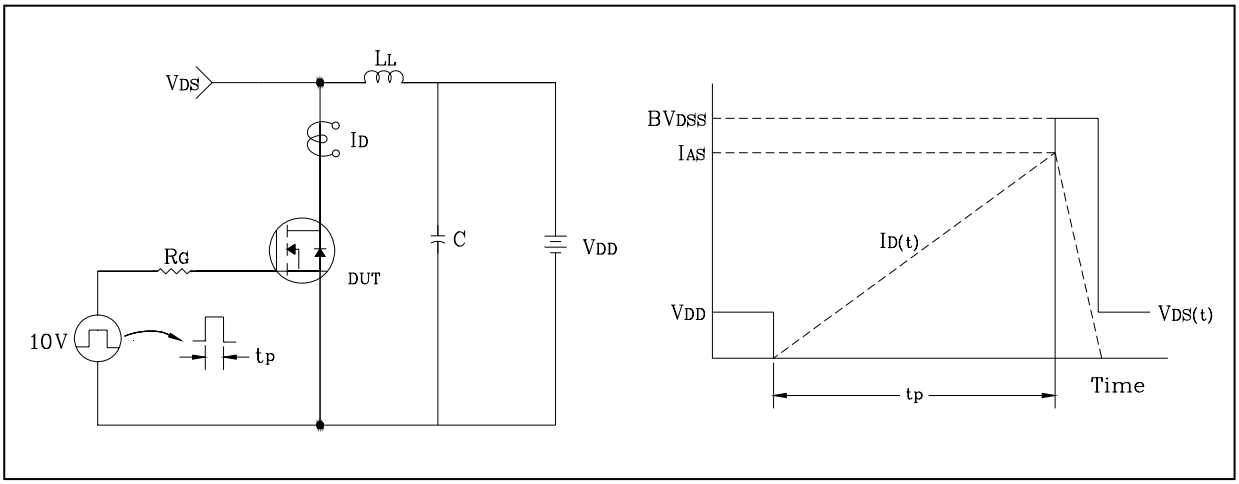
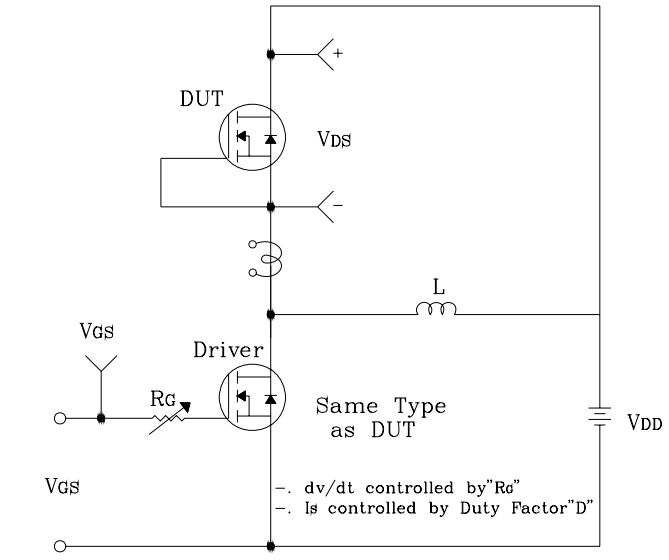
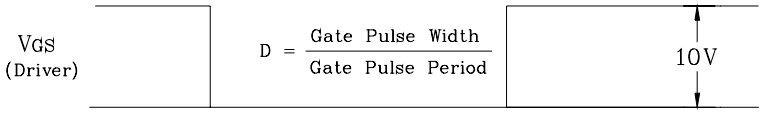
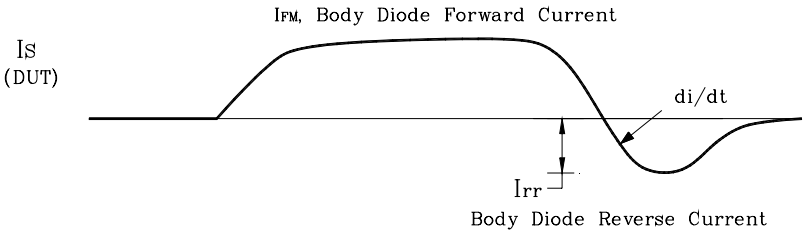
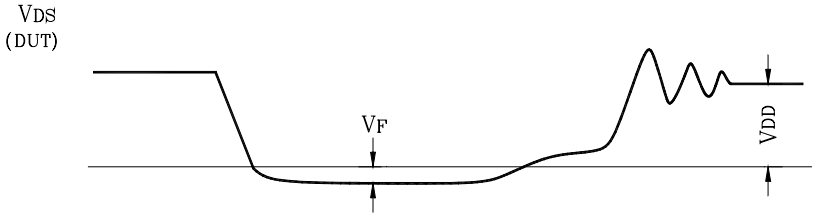


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



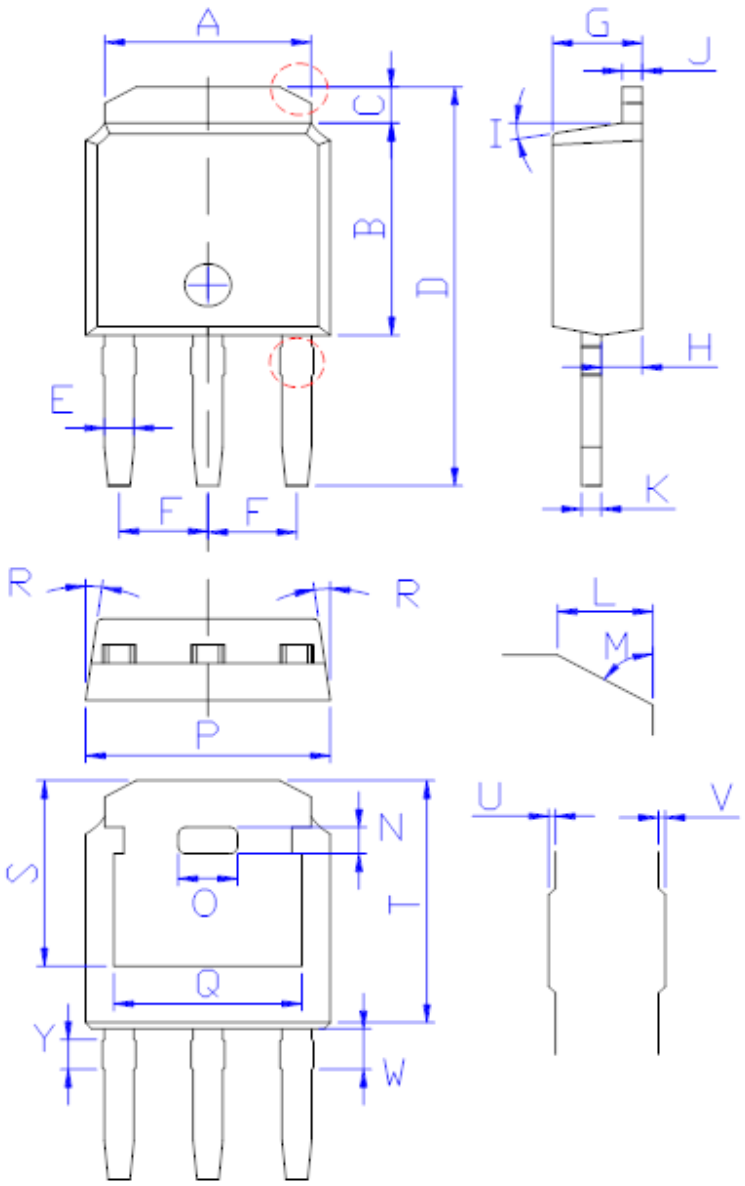






Outline Dimension

unit: mm



DIM	MILLIMETERS
A	5.34±0.30
B	6.00±0.30
C	1.05±0.30
D	11.31±0.30
E	0.76±0.15
F	2.28±0.15
G	2.30±0.30
H	1.06±0.30
I	(4-10)°
J	0.51±0.15
K	0.52±0.15
L	0.80±0.30
M	60°
N	0.75±0.30
O	1.80±0.30
P	6.60±0.30
Q	4.85±0.30
R	(4-8.5)°
S	5.30±0.30
T	6.90±0.30
U	0.05±0.05
V	0.05±0.05
W	1.15±0.25
Y	0.85±0.25

（单位：mm）